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PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

#15 / Req. for Reconsid 3/4/03 VShort

In re the Application of

Shoji TSUZUKI

Group Art Unit: 2823

Application No.: 09/671,884

Examiner: B. Kebede

Filed: January 10, 2001

Docket No.: 107927

For: CONNECTION SUBSTRATE, A METHOD OF MANUFACTURING THE CONNECTION SUBSTRATE, A SEMICONDUCTOR DEVICE, AND A METHOD OF MANUFACTURING THE SEMICONDUCTOR DEVICE

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REQUEST FOR RECONSIDERATION

Director of the U.S. Patent and Trademark Office
Washington, D.C. 20231

Sir:

In reply to the November 20, 2002 Office Action, reconsideration of the rejection is respectfully requested in light of the following remarks.

Claims 1-16 are pending in the present application. Claims 4, 10 and 16 have been withdrawn from consideration.

I. OBJECTION TO THE DRAWINGS UNDER 37 C.F.R. §1.83(a)

The Drawings are objected to because of informalities. Specifically, the Office Action asserts that the drawings do not show every feature of the invention specified in the claims 1, 5 and 11. Applicant respectfully traverses the objection to the drawings.

With respect to claim 1, "separating the metal wires and the insulation layer from the base" is shown from Fig. 4(4) to Fig. 5(1). Specifically, base 28 is illustrated in Fig. 4(4), and the base is separated from the structure in Fig. 5(1).

With respect to claim 5, "a step of separating the connection substrate from the base" is illustrated in the same figures as discussed above with respect to claim 1.

With regard to claim 11, "a step of separating the connection substrate from the second base" is illustrated from Fig. 5(3) to Fig. 5(4). Specifically, Fig. 5(3) shows base 36, and Fig. 5(4) illustrates base 36 separated from the structure.

Additionally, the drawings show "the base," as recited in claims 1-3 and 5-9, and "the first and second base," as recited in claims 11-15, respectively. Specifically, Figs. 3-5 illustrate a base/first base 28 and a second base 36. Accordingly, Applicant requests that the objection to the drawings be withdrawn.

II. REJECTION UNDER 35 U.S.C. §112, FIRST PARAGRAPH

Claims 1, 3, 5-9 and 11-15 were rejected under 35 U.S.C. §112, first paragraph as indefinite. This rejection is respectfully traversed.

The Office Action asserts that the specification does not reasonably provide enablement for "separating the metal wires and the insulation layer from the base," as recited in claim 1, line 9; "a step of separating the connection substrate from the base," as recited in claim 5, line 9; and "a step of separating the connection substrate from the second base," as recited in claim 11, line 12. This rejection is respectfully traversed.

Applicant respectfully asserts that the specification provides adequate support for these features on page 7, lines 11-19, indicated as paragraph 28; page 7, line 30 - page 8, line 5, indicated as paragraph 29; page 12, lines 12-25, in paragraph 47; and page 13, line 21-29, indicated as paragraph 50.

Specifically, with respect to claims 1 and 5, "separating the metal wires and the insulation layer from the base," and "a step of separating the connection substrate from the base" is enable by Fig. 5(1) and the specification, for example, paragraph 47. The specification indicates, "base 28 and the connection substrate 12 can be easily separated by irradiating light from a rear surface side of the first glass base 28."

Additionally, with respect to claim 11, "a step of separating the connection substrate from the second base is enable by Fig. 5(4) and, for example, paragraph 50. The disclosure of the claimed invention indicates that "the semiconductor device 10 is separated from the second glass base 36 (the separation method is the same as the first glass base 28)."

Applicant respectfully submits that claim 1-3, 5-9 and 11-15 fully comply with the requirements of 35 U.S.C. §112, first paragraph. Reconsideration and withdrawal of this rejection are respectfully requested.

III. REJECTION UNDER 35 U.S.C. §102(e)

Claims 1, 2, 5-7, 9, 11 and 13-15 were rejected under 35 U.S.C. §102(e) as unpatentable over U.S. Patent No. 5,977,641 to Takahashi (hereinafter "Takahashi"). This rejection is respectfully traversed.

Claim 1 recites a method of manufacturing a connection substrate in which the method includes a step of "separating the metal wires and the insulation layer from the base."

Claim 5 recites a method of manufacturing a semiconductor device in which the method includes "a step of separating the connection substrate from the base."

Claim 11 also recites a method of manufacturing a semiconductor device, the method including "a step of separating the first base from the connection substrate."

Contrary to the allegation set forth in the Office Action that Takahashi describes separating the base 1 from the other parts of the structure described therein, Takahashi in fact describes no such separating step.

More specifically, Takahashi describes a method of making a semiconductor device. As shown in Figs. 3A to 3C and Figs. 4A to 4C, and as described at col. 6, line 52 to col. 8, line 21, the method comprises forming a barrier metal layer 11 upon a semiconductor wafer 1 having electrode pads 15 previously formed therein. The barrier metal layer 11 is then selectively etched. An insulation layer 12 is then formed over the entire surface of the

substrate, but with openings left over the remaining portions of the barrier metal layer 11. Then, a metal layer to form a wiring pattern 13 is deposited and selectively etched. Finally, solder balls 14 as external electrodes are mounted on the land portions of the wiring pattern 13. The semiconductor device is then cut along the broken line in Fig. 4C in order to form semiconductor devices having a chip-size package structure including a ball grid array electrode.

The semiconductor wafer 1, upon which the remaining structure of the device is formed, is not separated from the remaining structure of the device following formation of the remaining structure, *see* in Figs. 3A to 3C and Figs. 4A to 4C.

Further, separating the semiconductor wafer 1 from the remaining structure of the device in Takahashi would completely destroy the device. The semiconductor wafer 1 in the Takahashi device is integral to the device and not merely a support substrate that may be removed as implied in the Office Action. For example, as explained at col. 6, lines 54-57 of Takashi, the semiconductor wafer 1 has formed thereon semiconductor elements, wires, a passivation film, electrode pads, etc. prior to the process steps illustrated in Figs. 3A to 4C. Accordingly, Takahashi indicates that the semiconductor wafer 1 is an integral, necessary part of the semiconductor device. Separating the semiconductor wafer 1 from the remaining structure of the device would destroy operation of the semiconductor device.

Finally, with particular respect to the method of claim 11, Takahashi also does not teach or suggest a process in which a connection substrate is disposed on a second base, separated from the first base, and ultimately separated from the second base as well. Contrary to the assertion in the Office Action, Takahashi fails to teach or suggest use of a second base as well.

Applicant respectfully submits that the rejection under 35 U.S.C. §102(e) should be withdrawn because Takahashi does not teach or suggest each feature of independent claims 1, 5 and 11 above.

For at least the foregoing reasons, reconsideration and withdrawal of this rejection are respectfully requested.

IV. REJECTION UNDER 35 U.S.C. §103(a)

Claims 3, 8 and 12 were rejected under 35 U.S.C. §103(a) as unpatentable over Takahashi. This rejection is respectfully traversed.

The Office Action alleges that it would been obvious to have used a glass substrate in place of the silicon semiconductor wafer 1 described in Takahashi based upon the allegation that "it is well-known in the art to use a glass substrate for packaging." This rejection is respectfully traversed.

Applicant respectfully submits that even if the above reasoning with respect to claims 3, 8 and 12 were to be accepted, such reasoning would still not remedy the additional deficiencies of Takahashi discussed extensively above. As discussed above, Takahashi discloses that a silicon semiconductor wafer must be used as an integral part of the semiconductor device described therein. Applicant respectfully submits that it is not at all evident that one of ordinary skill in the art would have replaced the silicon semiconductor wafer described in Takahashi with a glass substrate where the substrate is not to be removed from the rest of the structure as in Takahashi. Thus, one of ordinary skill in the art still would not have been led to the presently claimed invention from the teachings of Takahashi.

For at least the foregoing reasons, Applicant respectfully submits that one of ordinary skill in the art would not have been led to the presently claimed invention from the teachings of Takahashi. Additionally, the remainder of the claims that depend from independent claims 1, 5 and 11 are likewise distinguishable over the applied art for at least the reasons discussed

above, as well as for the additional features they recite. Reconsideration and withdrawal of this rejection are respectfully requested.

V. CONCLUSION

In view of the foregoing remarks, Applicant respectfully submits that this application is in condition for allowance. Favorable reconsideration and prompt allowance of claims 1-16 are earnestly solicited.

Should the Examiner believe that anything further would be desirable in order to place this application in even better condition for allowance, the Examiner is invited to contact the Applicant's undersigned representative at the telephone number listed below.

Respectfully submitted,

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Date: February 21, 2003

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